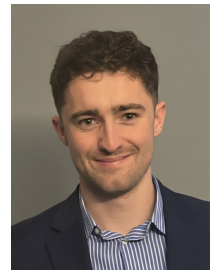


# CURRICULUM VITAE

## ELLIOTT QUÉRÉ

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### PROFESSIONAL EXPERIENCE

#### Doctoral Researcher

Université de Rennes / IRISA / INRIA — SUSHI Team (CentraleSupélec)

2024–Present

- Research on the security of heterogeneous **SoC–FPGA platforms** for cloud and edge computing, focusing on leakage risks from shared hardware resources and multi-tenant execution.
- Study of **microarchitectural behavior** through embedded power sensing rather than traditional timing analysis.
- Development of *MIRABELLE*, a framework combining on-chip sensing and signal processing to identify leakage sources invisible to software-only observation.
- Demonstrated that microarchitectural activity can be distinguished from on-chip power signatures without external probes.

#### Detection Engineer

Ministère des Armées, Rennes, France

2021–2024

- Designed graph-based models (Tid2Vec) to represent MITRE ATT&CK techniques and infer semantic relationships.
- Built an unsupervised Transformer-based pipeline for event-log analysis, including noise reduction and automatic pattern extraction.

#### Detection Engineering Intern

Apple Inc., London, United Kingdom

May–Sep. 2023

- Optimized large-scale security telemetry with Databricks and Apache Spark, reducing false positives in detection workflows.

#### Security Engineering Intern

Ministère des Armées, Rennes, France

Apr.–Jun. 2021

- Designed and deployed a multi-antivirus sandbox platform for malware detection and behavioral analysis.

### EDUCATION

#### Ph.D. in Hardware Security

Université de Rennes / IRISA / INRIA / SUSHI Team (CentraleSupélec)

Supervisors: Lilian Bossuet, Rubén Salvador, Maria Méndez Real, Alessandro Palumbo.

*PROACT Training School 2025 (Crete)*: hardware security, side-channel analysis, embedded cryptography.

*MICSEC 2025 International Winter School on Microarchitectural Security (Télécom Paris)*: cryptography, side channels and transient execution attacks, formal methods for security.

**Diplôme d'Ingénieur** in Telecommunications, Networks, and Computer Engineering 2021–2024  
IMT Atlantique, Brest, France — Specialization in Signal Processing.

- Research program: advanced musical source separation (segmentation models, Transformer ViT autoencoders).
- Project: modular FPGA synthesizer for frequency-domain processing and real-time sound synthesis.

#### Bachelor's Degree in Networks and Telecommunications

Université de Rennes — IUT de Saint-Malo, France

2019–2021

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**SKILLS**

**Programming:** C/C++, Python, Scala, Go, ARM Assembly  
**Hardware / FPGA:** Vivado, Vitis, Verilog, VHDL  
**Technologies:** Linux, Git, Docker, TensorFlow, PyTorch, Spark  
**Languages:** French (native), English (fluent), German (B1)

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**PUBLICATIONS**

E. Quéré, M. Mendez Real, A. Palumbo, L. Bossuet, R. Salvador, "Side-Channel Exploitation of DRAM Access Patterns for Fingerprinting FPGA–CPU Environments," *Proceedings of RESSI 2025 (Rendez-Vous de la Recherche et de l'Enseignement de la Sécurité des Systèmes d'Information)*, Lanniron, France, May 2025. [HAL: hal-05266486](https://hal.archives-ouvertes.fr/hal-05266486)

E. Quéré, L. Bossuet, R. Salvador, M. Mendez Real, A. Palumbo, "SNOOP+POWER: Remote Leakage of Coherence Decisions via On-Chip Power Observation," (in preparation).

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**PRESENTATIONS**

RESSI 2025 (Lanniron) — "DRAM Access Patterns and PDN Signatures," talk/poster.  
IRISA/SUSHI Group Seminars (2024–2025) — "SoC–FPGA Power Side-Channel Characterization."

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**TEACHING**

CentraleSupélec, Université Paris–Saclay (2024–2025)

- **Network Security (Bachelor's level):** lectures and hands-on tutorial labs.
- **Hardware Security and Digital Electronics (Bachelor/Master):** tutorials and FPGA design practicals.
- **Project Supervision (20 h):** impedance-based side-channel analysis on SoC — design, acquisition, and interpretation.

**Total teaching load:** 64 hours (2024–2025).